WHAT IS CLAIMED IS:

1. A read circuit which provides multi-bit disk data to a disk controller based on analog data from a disk head, said read circuit comprising:

a bit detector for providing single bit digital data corresponding to the analog data from the disk head, the bit detector being synchronized by a high frequency clock;

a synchronization mark detector for detecting a synchronization marker in response to said but detector; and

a clock generator for generating a lower-frequency clock from the high frequency clock with a phase adjustable in response to the synchronization mark detector.

2. A read circuit according to Claim 1, wherein said synchronization mark detector detects the synchronization marker based on the single bit data from said bit detector.

3. A read circuit according to Claim 1, wherein said high frequency clock is phase-locked to output of the disk head.

4. A read circuit according to Claim 1, further comprising an A/D converter for converting the analog data from the disk head to multi-bit digital data and providing such multi-bit digital data to said bit detector.

5. A read circuit according to Claim 4, wherein said A/D converter operates in synchronism with said high frequency clock.

6. A read circuit according to Claim 1, wherein said clock generator counts said high frequency clock and adjusts phase of the lower-frequency clock by a reset of the count.

7. A read circuit according to Claim 1, wherein said clock generator comprises a resettable divider for dividing said high frequency clock, and a cycle counter for monitoring a count of said high frequency clock, wherein said cycle counter is responsive to said synchronization mark detector to generate a reset signal for said resettable divider in accordance with whether said divider is in a first half cycle or a second half cycle.

8. A method for providing multi-bit disk data to a disk controller based on analog data from a disk head, said method comprising:

detecting single bit digital data in synchronism with a high frequency clock, said detecting step detecting the single bit digital data in correspondence to the analog data from the disk head;

detecting a synchronization mark based on the single bit digital data; and

generating a lower-frequency clock from the high frequency clock, the lower-frequency clock having a phase adjustable in response to the detection of the synchronization mark.

9. A method according to Claim 8, wherein said high frequency clock is phase-locked to output of the disk head.

10. A method according to Claim 8, wherein said detecting step comprises analog-to-digital conversion of the analog data from the disk head to multi-bit digital data and detection of the single bit digital data in such multi-bit digital data.

11. A method according to Claim 10, wherein said A/D conversion operates in synchronism with the high frequency clock.

12. A method according to Claim 8, wherein said generating step counts the high frequency clock and adjusts phase of the lower-frequency clock by a reset of the count.

13. A method according to Claim 8, wherein said generating step comprises division of the high frequency clock by a resettable divider and monitoring a count of said high frequency clock, wherein said resettable divider is reset in accordance with whether said synchronization mark occurs while said divider is in a first half cycle or a second half cycle.

14. A read circuit which provides multi-bit disk data to a disk controller based on analog data from a disk head, said read circuit comprising:

bit detector means for providing single bit digital data corresponding to the analog data from the

disk head, the bit detector means being synchronized by a high frequency clock means;

synchronization mark detector means for detecting a synchronization marker in response to the single bit digital data; and

clock generator means for generating a lower-frequency clock from the high frequency clock means with a phase adjustable in response to the synchronization mark detector means.

15. A read circuit according to Claim 14, wherein said synchronization mark detector means detects the synchronization mark based on the single bit from said single bit detector means.

16. A read circuit according to Claim 14, wherein said high frequency clock means is phase-locked to output of the disk head.

17. A read circuit according to Claim 14, further comprising A/D converter means for converting the analog data from the disk head to multi-bit digital data and providing such multi-bit digital data to said bit detector means.

18. A read circuit according to Claim 18, wherein said A/D converter means operates in synchronism with said high frequency clock means.

19. A read circuit according to Claim 14, wherein said clock generator means counts said high

frequency clock means and adjusts phase of the lower-frequency clock by a reset of the count.

20. A read circuit according to Claim 14, wherein said clock generator means comprises resettable divider means for dividing said high frequency clock means, and cycle counter means for monitoring a count of said high frequency clock means, wherein said cycle counter means is responsive to said synchronization mark detector means to generate a reset signal for said resettable divider means in accordance with whether said divider means is in a first half cycle or a second half cycle.

21. A read circuit according to Claim 1, further comprising a high frequency clock.

22. A read circuit according to Claim 14, further comprising high frequency clock means.

23. A disk drive comprising:

a disk head;

a disk controller; and

a read circuit which provides multi-bit disk data to the disk controller based on analog data from the disk head, said read circuit comprising:

a bit detector for providing single bit digital data corresponding to the analog data from the disk head, the bit detector being synchronized by a high frequency clock;

a synchronization mark detector for detecting a synchronization marker in response to said but detector; and

a clock generator for generating a lower-frequency clock from the high frequency

clock with a phase adjustable in response to the synchronization mark detector.

24. A disk drive according to Claim 23, wherein said synchronization mark detector detects the synchronization marker based on the single bit data from said bit detector.

25. A disk drive according to Claim 23, wherein said high frequency clock is phase-locked to output of the disk head.

26. A disk drive according to Claim 23, further comprising an A/D converter for converting the analog data from the disk head to multi-bit digital data and providing such multi-bit digital data to said bit detector.

27. A disk drive according to Claim 26, wherein said A/D converter operates in synchronism with said high frequency clock.

28. A disk drive according to Claim 23, wherein said clock generator counts said high frequency clock and adjusts phase of the lower-frequency clock by a reset of the count.

29. A disk drive according to Claim 23, wherein said clock generator comprises a resettable divider for dividing said high frequency clock, and a cycle counter for monitoring a count of said high frequency clock, wherein said cycle counter is responsive to said synchronization mark detector to generate a reset signal for said resettable divider in

accordance with whether said divider is in a first half cycle or a second half cycle.

30. A disk drive comprising:

a disk head means for writing/reading data to/from a disk;

a disk controller means for controlling the disk drive; and

a read circuit means for providing multi-bit disk data to the disk controller means based on analog data from the disk head means, said read circuit means comprising:

bit detector means for providing single bit digital data corresponding to the analog data from the disk head, the bit detector means being synchronized by a high frequency clock means;

synchronization mark detector means for detecting a synchronization marker in response to the single bit digital data; and

clock generator means for generating a lower-frequency clock from the high frequency clock means with a phase adjustable in response to the synchronization mark detector means.

31. A disk drive according to Claim 30, wherein said synchronization mark detector means detects the synchronization mark based on the single bit from said single bit detector means.

32. A disk drive according to Claim 30, wherein said high frequency clock means is phase-locked to output of the disk head.

33. A disk drive according to Claim 30, further comprising A/D converter means for converting the analog data from the disk head to multi-bit digital data and providing such multi-bit digital data to said bit detector means.

34. A disk drive according to Claim 33, wherein said A/D converter means operates in synchronism with said high frequency clock means.

35. A disk drive according to Claim 30, wherein said clock generator means counts said high frequency clock means and adjusts phase of the lower-frequency clock by a reset of the count.

36. A read disk drive according to Claim 30, wherein said clock generator means comprises resettable divider means for dividing said high frequency clock means, and cycle counter means for monitoring a count of said high frequency clock means, wherein said cycle counter means is responsive to said synchronization mark detector means to generate a reset signal for said resettable divider means in accordance with whether said divider means is in a first half cycle or a second half cycle.

37. A disk drive according to Claim 23, further comprising a high frequency clock.

38. A disk drive according to Claim 30, further comprising high frequency clock means.